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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,500	03/31/2004	Neal Wolff	42P17272	1301

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,500	WOLFF ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/815,500, filed 03/31/2004. Claims 1-39 are presently under examination and pending in the Application.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "frequency divider" recited in claims 10, 11, 20 and 21 must be shown or the feature canceled from the claims.

Also, the drawings fail to show reference characters or numerical designations for the "clocked circuit" described in the specification and recited in the claims. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-23 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: There is no structural cooperative relationship for "the phase locked loop output", because it is unclear how the "phase locked loop" receives an input signal. Also, there is no structural cooperative relationship for "a first phase locked loop", since the loop output is not connected to any of the elements recited in the claims. Further, there is no structural cooperative relationship for "the second phase locked loop output", since the loop output is not connected to any of the elements recited in the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 9-11, 13-16, 24-26, 28-34 and 36-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Wyatt (US Patent No: 7,002,358), filed: December 10, 2003.

Regarding independent Claims 1, 24, 32, Wyatt discloses an apparatus and method for measuring jitter, which includes generating a jitter pulse having a width corresponding to an amount of jitter, Figs. 2 and 5, comprising:

A reference input port (CLK1 212) in an integrated circuit 200 to receive a reference clock (waveform A, Fig. 1) based on an external clock, such as a bypass clock, Fig. 2.

A feedback input port (CLK2 214) in the integrated circuit 200 to receive a feedback clock (CLK2 214) from a clocked circuit (PLL 520) from the feedback divider 528.

A logic comprising phase/frequency detector 210 coupled to the pulse difference generator 220 to compare the reference clock (CLK1 212) and feedback clock (CLK2 214), and to generate a "jitter pulse", UP_DN 222 signal, having a width corresponding to the absolute value of the difference between the UP_L and DN_L pulse widths, as shown Fig. 2.

Regarding Claims 2, 25, 33, Wyatt discloses a reference clock (waveform A, Fig. 1), is based on clock signal, such as a bypass clock, which is external to the integrated circuit 200, Fig. 2.

Regarding Claim 3, Wyatt discloses a PLL 520, which generates the feedback clock (CLK2 214), Fig. 5.

Regarding Claims 4, 13, 14, 26, 34, Wyatt discloses a "jitter pulse", UP_DN 222 signal having a width corresponding to an amount of jitter, indicating that the reference clock and the feedback clock are not aligned. When the PLL_LOCK 268 signal transitions high, then it indicates that CLK1 and CLK2 are synchronized. The PLL_LOCK 268 signal is used in FIG. 2 to generate the INIT 266 signal, which controls the selection of multiplexer 230 for PWGOOD or UP_DN signals, Fig. 2. The jitter pulse is applied to the signal in (SI) input of the first latch 240. The first latch trims a pre-determined amount from the received jitter pulse to form a modified pulse at the signal out (SO) output of the first latch. The SI input of each successive latch is coupled to the SO output of the previous latch.

Regarding Claim 9, Wyatt discloses jittered clock edge 122, which lags reference clock edge 112 by a displacement $\Delta T1$. Jittered clock edge 124 leads reference clock

edge 114 by a displacement ΔT2. Generally, for a given clock edge location 116, the jittered clock edge will occur in a region 140 near the corresponding reference clock edge location. For any given clock cycle, the jittered clock edge location bears a statistical relationship to the ideal location (i.e., the corresponding reference clock edge transition) as indicated by probability distribution function 130, shown in Fig. 1.

Regarding Claims 10, 11, 28-31, 35-39, Wyatt discloses reference clock (waveform A, Fig. 1) is based on clock signal, such as a bypass clock, which is external to the integrated circuit 200, Fig. 2. The reference clock can be generated externally at a frequency lower than the bypass clock, utilizing a frequency divider including a counter, which are inherent devices utilized in frequency division of a clock. Regarding Claims 15, 16, Wyatt discloses a typical PLL 520, which includes a phase detector 522, a loop filter 524, a voltage controlled oscillator, and a feedback loop 529 that may include a feedback divider 528 for generating a CLOCK OUT 530 that is a fraction of the reference clock, CLK1 510. The input reference clock, CLK1 510 is provided as CLK1 212 in FIG. 1. CLK2 214 of FIG. 2 is taken from the feedback loop 529 after any feedback elements. The PLL 520 also provides a phased loop locked signal, PLL_LOCK 268 that is low until phase detector 522 determines that the phase /frequency difference between CLK1 510 and CLK2 214 is less than a lock threshold. In such a case, the PLL_LOCK 268 signal transitions high to indicate that CLK1 and CLK2 are synchronized, Fig. 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8,12,17-23,27 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wyatt (US Patent No: 7,002,358) in view of Cox et al. (US Patent No: 6,583,679), filed: June 28, 2001.

Regarding Claims 5-8, 12, 27, Wyatt does not explicitly disclose pulse suppression signal to suppress a portion of the bypass clock. In analogous art, Cox discloses a pulse deletion logic 230 which produces a pulse deletion control signal 231, which is gated with a signal carrier signal 221, using an "AND" gate 232, which produces signal 361 having missing (deleted) pulses, Figs 3a and 3b. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a pulse deletion logic in the apparatus of Wyatt, as taught by Cox, for the purpose of eliminating unwanted pulses in Wyatt's reference clock due to jittering, since deleting a single pulse impacts phase noise (jitter) effectively causing least phase distortion at moments of greatest amplitude.

Regarding independent Claim 17, Wyatt discloses a system for measuring jitter, which includes generating a jitter pulse having a width corresponding to an amount of jitter, Figs. 2 and 5, comprising:

A voltage controlled crystal oscillator (VCO) which is external to integrated circuit 200 to generate a primary clock (CLK1 212), also shown as (waveform A), Figs. 1, 2 and 5, and a first phase locked loop (PLL 520) input 510 to receive the primary clock (CLK1 212),

A second phase locked loop input (CLK2 214) to receive the feedback clock (CLK2 214) from the (PLL 520) from the feedback divider 528.

Logic comprising phase/frequency detector 210 coupled to the pulse difference generator 220 to compare the reference clock (CLK1 212) and feedback clock (CLK2 214), and to generate a "jitter pulse", UP_DN 222 signal, having a width corresponding to the absolute value of the difference between the UP_L and DN_L pulse widths, as shown Fig. 2.

Wyatt does not explicitly disclose a bypass gate to select the synchronized clock or a bypass clock. In analogous art, Cox discloses a pulse deletion logic 230 which produces a pulse deletion control signal 231, which is gated with a signal carrier signal 221, using an "AND" gate 232, which produces signal 361 having missing (deleted) pulses, Figs. 3a and 3b. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a pulse deletion logic in the apparatus of Wyatt, as taught by Cox, for the purpose of eliminating unwanted pulses in Wyatt's

reference clock due to jittering, since deleting a single pulse impacts phase noise (jitter) effectively causing least phase distortion at moments of greatest amplitude.

Regarding Claims 18-23, Wyatt discloses a "jitter pulse", UP_DN 222 signal having a width corresponding to an amount of jitter, indicating that the reference clock and the feedback clock are not aligned. When the PLL_LOCK 268 signal transitions high, then it indicates that CLK1 and CLK2 are synchronized. The PLL_LOCK 268 signal is used in FIG. 2 to generate the INIT 266 signal, which controls the selection of multiplexer 230 for PWGOOD or UP_DN signals, Fig. 2. The jitter pulse is applied to the signal in (SI) input of the first latch 240. The first latch trims a pre-determined amount from the received jitter pulse to form a modified pulse at the signal out (SO) output of the first latch. The SI input of each successive latch is coupled to the SO output of the previous latch.

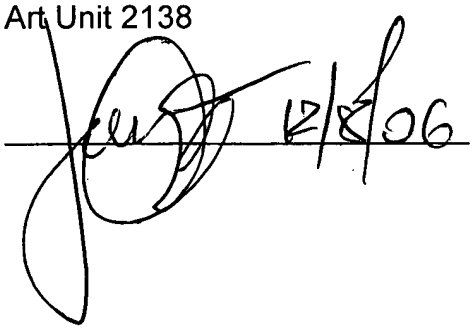
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



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